What is claimed is:

1. A test data compression method comprising steps of:

(a) finding compatible inputs and inversely compatible inputs using given test data T_D;

(b) generating a compression code based on a statistical coding;

(c) replacing unspecified bits ('X' values) of the test data with specific values chosen to maximize compression of the test data;

(d) re-ordering a sequence of patterns of the test data to generate as many instances as possible of the bit pattern to be compressed based on the size of the blocks; and

(e) compressing the blocks using the compression code,

wherein the compression code is generated in such a manner that only one recurring 4-bit pattern that has the highest frequency of appearance is compressed into a 1-bit compression code and the other bits are grouped into blocks consisting of a 2-bit codeword, the 2-bit codeword blocks having the original values of the bits.

2. The test data compression method as claimed in claim 1, wherein the step (a) comprises the steps of:

preparing an input check set C and initializing $C_i(0 \le i \le N-1)$ to UNIQUE (UNIQUE means that an input i is not compatible or inversely compatible);

detecting compatibility between an input $v(i,k)$ and a comparison input $v(j,k)$ over the entire test sequence $k(0 \le k \le L-1)$ of the given test data T_D using a function is compatible; and

confirming whether there are values that conflict with previous other compatible inputs or inversely compatible inputs using a function conflict check within the function is compatible if the input $v(i,k)$ or $v(j,k)$ has an 'X' value (don't care).

3. The test data compression method as claimed in claim 1, wherein the step (c) replaces all the 'X' values with '0's such that the patterns have a lot of '0's, the step (d) includes a step of storing the first value and the last value of each test data pattern in which 'X' values have been replaced with '0's and previously calculating the length of the pattern and a step of making the last value of each pattern become identical to a value of the next pattern and re-ordering the sequence of the patterns to generate as many instances as possible of the block to be compressed , so that a block having consecutive '0's can frequently appear, and the step (e) selects and compresses one block having the highest frequency of appearance using the compression code generated in the step (b).

4. A test data decompression apparatus including a controller that decompresses test data compressed by the test data compression method as claimed in claim 1, inputs the decompressed test data to a scan chain in the tested device, and controls signals transmitted between an ATE and an FSM, comprising:

an FSM decoder that includes inputs, one of which is a test clock input and the other an input to which the compressed test data is transmitted from a channel of a tester, and outputs, one of which is a data output port through which original data obtained when the compressed data is decompressed is transmitted and the other an output port through which control signals are output; and

a serializer that inputs the decompressed test data to the scan chain in synchronization with an FSM clock of the FSM decoder and a chip test clock.

5. The test data decompression apparatus as claimed in claim 4, wherein the control signals include a signal "parallel load (Par.)", a signal "serial load (Ser.)" and a signal "Wait", when the

first bit of the compression bit is '1', which represents an uncompressed pattern, the decoder transmits subsequent bits and the control signal "serial load (Ser.)" to the serializer for two clock cycles, and when the first bit of the compression bit is '0', which indicates one compressed block, the decoder delivers P_0 corresponding to bits of the corresponding block and the control signal "parallel load(Par.)" in parallel to the serializer.

6. A test data decompression apparatus including a controller that decompresses test data compressed by the test data compression method as claimed in claim 2, inputs the decompressed test data to a scan chain in the tested device, and controls signals transmitted between an ATE and an FSM, comprising:

an FSM decoder that includes inputs, one of which is a test clock input and the other an input to which the compressed test data is transmitted from a channel of a tester, and outputs, one of which is a data output port through which original data obtained when the compressed data is decompressed is transmitted and the other an output port through which control signals are output; and

a serializer that inputs the decompressed test data to the scan chain in synchronization with an FSM clock of the FSM decoder and a chip test clock.

7. The test data decompression apparatus as claimed in claim 6, wherein the control signals include a signal "parallel load (Par.)", a signal "serial load (Ser.)" and a signal "Wait", when the first bit of the compression bit is '1', which represents an uncompressed pattern, the decoder transmits subsequent bits and the control signal "serial load (Ser.)" to the serializer for two clock cycles, and when the first bit of the compression bit is '0', which indicates one compressed block, the decoder delivers P_0 corresponding to bits of the corresponding block and the control signal

"parallel load(Par.)" in parallel to the serializer.

8. A test data decompression apparatus including a controller that decompresses test data compressed by the test data compression method as claimed in claim 3, inputs the decompressed test data to a scan chain in the tested device, and controls signals transmitted between an ATE and an FSM, comprising:

an FSM decoder that includes inputs, one of which is a test clock input and the other an input to which the compressed test data is transmitted from a channel of a tester, and outputs, one of which is a data output port through which original data obtained when the compressed data is decompressed is transmitted and the other an output port through which control signals are output; and

a serializer that inputs the decompressed test data to the scan chain in synchronization with an FSM clock of the FSM decoder and a chip test clock.

9. The test data decompression apparatus as claimed in claim 8, wherein the control signals include a signal "parallel load (Par.)", a signal "serial load (Ser.)" and a signal "Wait", when the first bit of the compression bit is '1', which represents an uncompressed pattern, the decoder transmits subsequent bits and the control signal "serial load (Ser.)" to the serializer for two clock cycles, and when the first bit of the compression bit is '0', which indicates one compressed block, the decoder delivers P_0 corresponding to bits of the corresponding block and the control signal "parallel load(Par.)" in parallel to the serializer.